Revision

to

DNA EMP PREFERRED TEST PROCEDURES

(DNA 3286H)

February 1977

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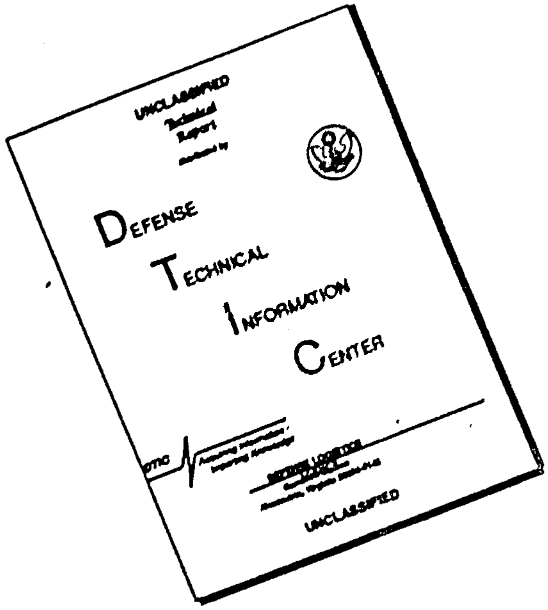

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

EMP Hardening
EMP Tests
EMP Hardening Component
EMP Surge Arresters
EMP Filters
EMP Specification
EMP Current Injection
EMP Modular/Subsystem Tests
EMP Upset/Damage
Surge Arrester Characterization

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

EMP preferred test procedures are provided to evaluate and characterize the performance of:

1) filters
2) surge arresters
3) gaskets
4) vents
5) coaxial cables & connectors
6) shielded enclosures
7) conduit systems
8) transformers and inductors
9) resistors

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6. PERFORMING ORG. REPORT NUMBER (Continued)

and E6323

19. KEY WORDS (Continued)

Filter Characterization
EM Gaskets
EM Vents
Coaxial Cable Shields
Shielded Coaxial Connectors
Shielded Enclosures
Shielded Rooms
Conduits
Resistor Damage
Capacitor Damage
Inductor Damage
Transformer Damage
Resistor Characterization
Inductor Characterization
Surge Arrester Damage
Filter Damage
Gasket Shielding Characterization
Surface Transfer Impedance
Surface Transfer Admittance
E-Field Shielding Effectiveness
H-Field Shielding Effectiveness
Conduit Couplers
Capacitor Characterization
Transformer Characterization

20. ABSTRACT (Continued)

10) capacitors
11) electronic modules
12) computers
13) analog modules

Topics covered are experiment design, documentation, typical induced EMP transients, current injection testing, and the specific test procedures to evaluate the EMP behavior for each type of electronic component.

SUMMARY

IIT Research Institute, under contract to the Defense Nuclear Agency (DNA001-72-C-0084, DNA001-73-C-0149 and DNA001-75-C-0201), has developed EMP PREFERRED TEST PROCEDURES for selected electronic components. This is part of a continuing program to formulate and recommend procedures by which EMP test data may be obtained and reported.

In this connection, it is important to realize what these preferred procedures are and what they are not. They are a formal recognition of good practices and methods based on sound physical principles which can lead to useful EMP data. They provide a means of communicating useful information among workers in a large multidisciplined technology.

These preferred procedures are not necessarily cook-book simplifications and are not intended to be a "MIL-SPEC" or a panacea for designers of hardened systems. The EMP PREFERRED TEST PROCEDURES require some experience and intelligence on the part of the experimenter. These are somewhat different than "MIL-SPEC" testing which can usually be implemented by a responsible technician. The procedures emphasize the electrical test aspects. Some general guidance as to limits and other environmental aspects is provided; however, these are more properly considered in terms of the requirements for a specific system, such as design specifications. The procedures are designed to employ readily available or easily constructed laboratory equipment--generally operating below 100,000 volts and 100 MHz--and to be conducted in ordinary room-size laboratory space.

The material contained in this document is considered the best available and, where possible, it represents a concensus of recognized practices. Based on discussions with prominent members of the EMP commuity as well as other experts, preliminary outlines of the procedures were devised and actual tests conducted to validate the procedures. A draft of the procedures was then circulated among cognizant professionals in a number of organizations, and revised as needed to

harmonize various viewpoints. While the results in this document are based on the experience of a number of active recognized professionals, it must be noted that all possible situations could not be considered. Clearly, it is not the intent of this document to impose "National EMP Standards and Limits." Even if these were desirable, it would not be appropriate to do so today because of the rapid changes taking place in the state-of-the-art. In this regard, it is important that others take an active part in supplying additional information to effect improvements.

Much of the work presented in the first three sections in this edition of the EMP PREFERRED TEST PROCEDURES was summarized directly from DNA Document 2028H, entitled "TREE Preferred Procedures." IIT Research Institute, therefore, gratefully acknowledges the efforts of Mr. Richard H. Thatcher and Mr. Michael L. Green at the Battelle-Columbus Laboratories for their efforts on DNA 2028H.

Discussions were also held with staff members of a number of organizations in EMP hardening. All organizations cannot be acknowledged, but include U.S. Army Electronics Command, Picatinny Arsenal, Naval Surface Weapons Center, Harry Diamond Laboratories, Defense Civil Protection Agency, Construction Engineering Research Laboratory, Boeing Aircraft Corporation, Lockheed Corporation, International Rockwell, General Semiconductor Industries, Siemens Corporation, Signalite, Joslyn Electronic Systems, Electro-Data Technology, Sandia Laboratory, and Stanford Research Institute.

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15. TEST PROCEDURES FOR CURRENT INJECTION FOR ELECTRONIC MODULES

15.1 Introduction

15.1.1 Purpose

The purpose of this chapter is to provide a guidelines for interim preferred EMP test procedures to determine the effects of EMP induced voltage/current transients on modular equipment. No new procedures have been developed under this program and it is assumed that future work in the EMP testing area will produce new and better techniques.

Throughout, the emphasis is on simplicity and on the use of readily available laboratory instruments. A major objective in this effort has been to review and evaluate the many existing EMP test techniques and select the minimum set necessary to satisfy the needs of many different users. Thus, the procedures described here are a subset of the EMP test methods currently in use.

15.1.2 Scope

There are two major aspects to determining the effects of EMP current/voltage transients on modular equipments, i.e., (1) inducing the EMP transient, and (2) detecting/measuring the effect(s) of that transient. Since the techniques required to detect and measure these effects are determined by the function of the specific module and since this chapter is concerned with the EMP testing of modules in general, the topic of detection and measurement is beyond the scope of this chapter. Techniques for detection and measurement of the effects must be developed by an individual familiar with the function and circuitry of the specific module. Thus, this chapter is concerned only with the techniques required to produce the effects of EMP induced transients as accurately as possible.

The principal topics to be considered include the simulation of EMP waveforms, methods of introducing the simulated pulses

into the module, techniques for terminating cables connected to the modules and means of synchronizing the pulse delivery with operation of a multi-state unit under test.

The many techniques currently in use have been surveyed through discussion with a number of companies currently involved in EMP testing and evaluated by running a battery of tests on each of three representative modules.

As many test techniques as possible have been examined.* Two methods have been used to introduce the EMP:

- Bulk-current injection
- Direct (pin-to-case) injection.

In the direct injection method several different waveshapes were utilized:

- $\pm$ square pulses
- CW RF
- Damped RF sinusoids (Figure 15.2B)
- RF burst (Figure 15.3B).

The representative modules used to evaluate the EMP test techniques were:

- A Nova 1220 minicomputer
- A HP-462 broadband RF preamplifier
- A HP-6429 dc power supply.

These units represent digital, in-EMP-band analog, and out-of-EMP band analog equipment, respectively. For digital equipment, various terminal conditions, such as high impedance versus low impedance, were investigated.

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* Free field EMP pickup tests have not been considered, as such tests are a measure of the quality of the enclosure rather than the module. Enclosure testing is covered in Chapter 10.

15.2 Module Testing to EMP Specifications

15.2.1 Applicability

This type of testing is applicable to testing programs with any of the following objectives:

- Verifying the hardness of each module terminal to a specified EMP.
- Providing data for hardening design/redesign.
- Providing data to identify failures within the module due to a specified EMP.
- Verifying overall module hardness to a specified EMP (i.e., system level testing) when the methods of Section 15.4 are not practical.

At present, module testing to EMP specification is the principal type of EMP testing being done. The magnitudes and spectral contents of the injected signals are specified by the Program Office for the system in which the module is being utilized. Generally, the specifications take one of two formats:

- Pin-to-case voltage/current specification
- Bulk current specification.

The Direct Pulse Injection test, Section 15.2.2 shall be used for this type of testing. Pin-to-case injection is recommended. Thus, pin-to-case specifications automatically describe the required frequencies and amplitudes for the test pulses.

Bulk current specifications, however, require conversion to a pin-to-case format. For high impedance terminations, it has been shown[1] that a good rule of thumb for determining worst case terminal voltages, given a bulk current, is to multiply the specified bulk current by 100 V/A, i.e., given a bulk current of 3 amperes, the voltage appearing between the module terminals and the case will be 300 volts or less. For low impedance terminations (where impedance $< 100\Omega$), current becomes the limiting factor such that the pulse current shall not exceed the specified bulk current. Thus, for the

example 3 ampere bulk current, the simulated EMP pulses are to be limited to 300 volts or 3 amperes, whichever occurs first.

For balanced inputs/outputs, pin-to-pin injection shall also be utilized. However, maximum pin-to-pin pulse voltage shall be reduced to 20 dB below the maximum pin-to-case voltage determined above. Every pin should be tested except in cases of extreme redundancy, such as a computer data bus. In such cases, it is necessary to test only two or three lines to insure that the effects are the same for all.

15.2.2 Direct Pulse Injection Test Procedures

15.2.2.1 Scope

Direct pulse injection tests are used to determine the effects of EMP transients on electronic modules at a fairly detailed level (i.e., for each terminal).

As discussed in the Introduction, this chapter is concerned primarily with providing techniques for simulating EMP transients and for introducing these transients into the module in a fashion that will duplicate the effects of an actual EMP as accurately as possible. Methods for detecting and measuring these effects are discussed only in the general case.

15.2.2.2 Test Equipment and Setup

Figure 15.1 illustrates the basic test setup for generating and introducing simulated EMP transients onto the terminals of a module.

A signal source, which is discussed in greater detail below, is used to produce the desired transient waveshape. This signal is amplified to the required level by a broadband RF power amplifier. This amplifier should have a power rating of at least 100 watts and a frequency range of approximately 10 kHz to 200 MHz. The IFI 402 is an example of such an amplifier.

The output of the amplifier is the simulated EMP which is coupled to the terminal of interest. This simulated EMP may

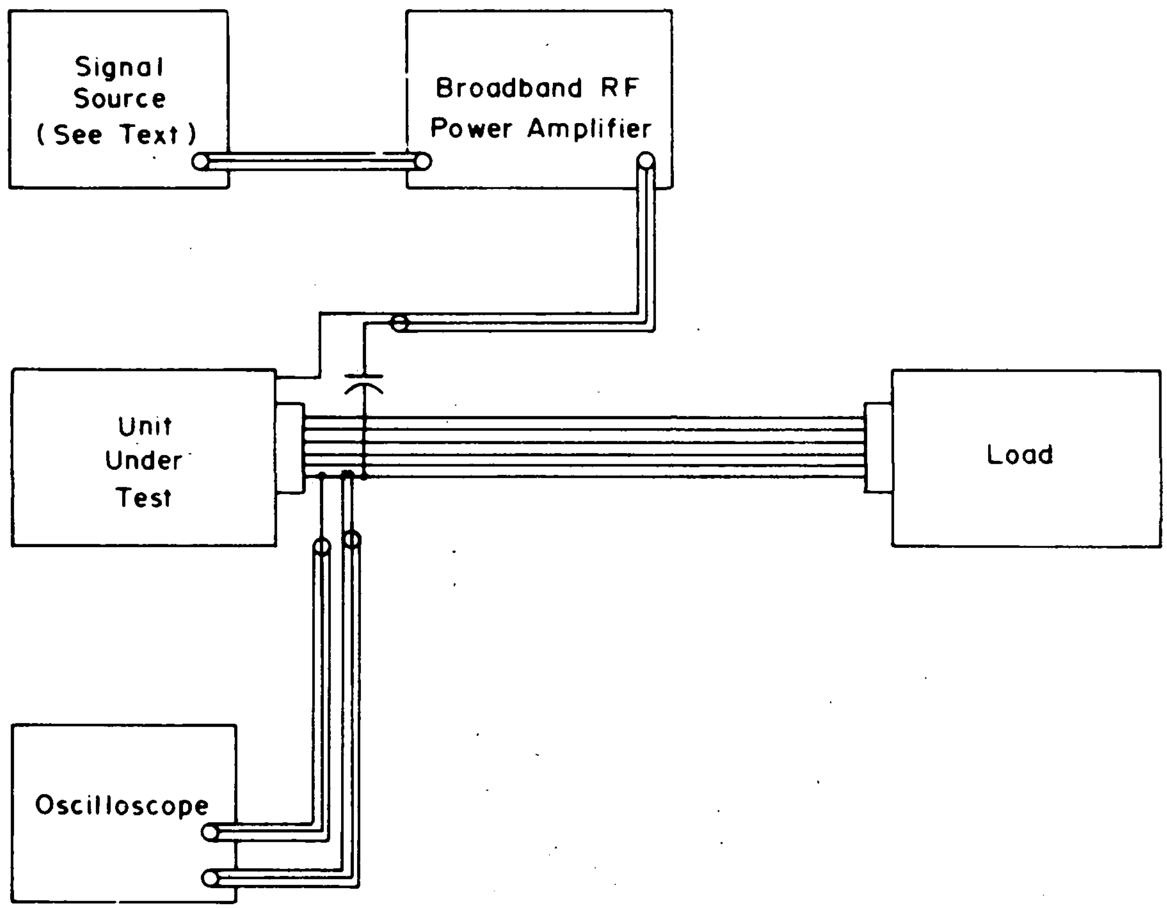


Fig. 15.1 BASIC DIRECT INJECTION TEST SETUP

be coupled onto the terminal capacitivly as shown in Figure 15.1, inductively (i.e., with a current transformer) or directly.

The module is to be tested in an operational state, i.e., energized and functioning. Thus, it is necessary to terminate the cable from the unit under test. Ideally, the actual unit(s) that would terminate the cable in a real system should be used as the load. In reality, this is often impossible since the actual load units may be unknown, unavailable or sensitive to EMP transients. In such cases it is necessary to simulate the actual or anticipated load impedances, voltage levels, control signals, etc., to the unit under test. Load impedances generally may be simulated with simple RC networks. The simulation of voltage levels or control signals, however, requires the attention of someone familiar with the unit under test.

A dual beam oscilloscope should be used to monitor the transient voltage and current on the terminal being tested.

Figure 15.2A illustrates the equipment setup for generating damped RF sinusoids. A typical waveform and its associated spectral distribution are shown in Figures 15.2B and 15.2C, respectively. This waveform may be used for damage or upset testing.

An RF generator, such as the HP8601A, is used to provide CW RF. This unit is set to the desired test frequency.

For upset testing, the RF (AUX in Figure 15.2A) may be used to trigger the pulser; however, it is necessary to use some timing or counting circuits (shown as optional trigger) so that the EMP transients will be generated at a low duty cycle. A repetition rate of 1 kHz is suitable.

Alternately, the pulser may be free running at a repetition rate of 1 kHz. This method is simpler but does not synchronize the pulser (i.e., the double exponential envelope) with the RF.

For damage testing, the pulser should be operated single shot.

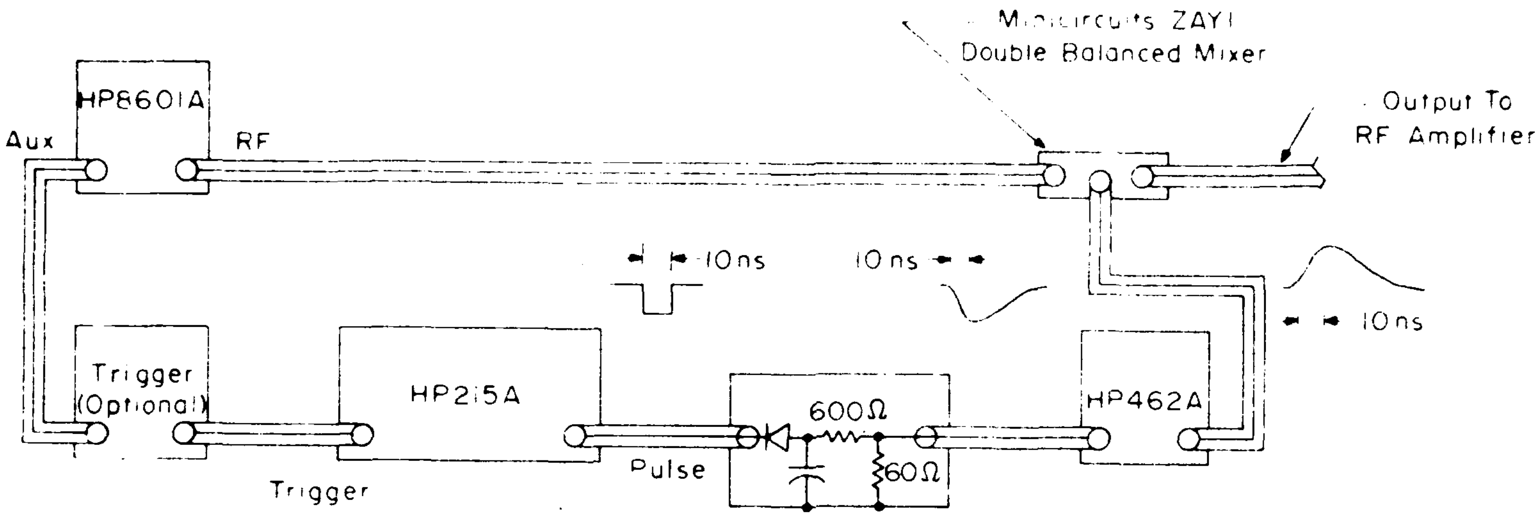


Fig. 15.2A TYPICAL TEST SETUP FOR GENERATING DAMPED SINUSOIDS

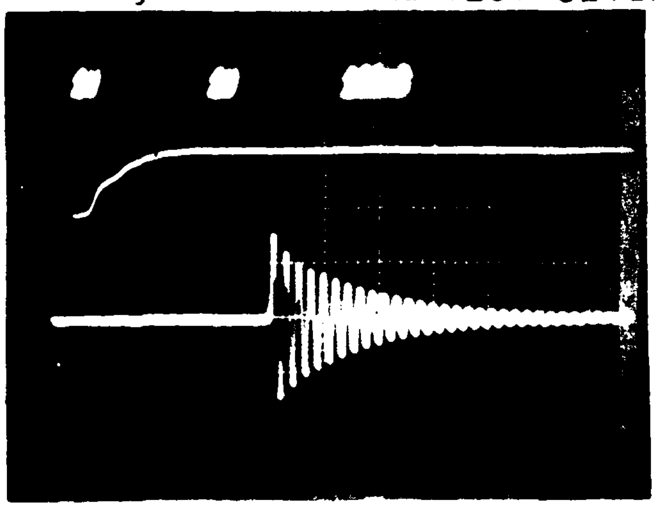


Fig. 15 2B DAMPED SINUSOID WAVEFORM

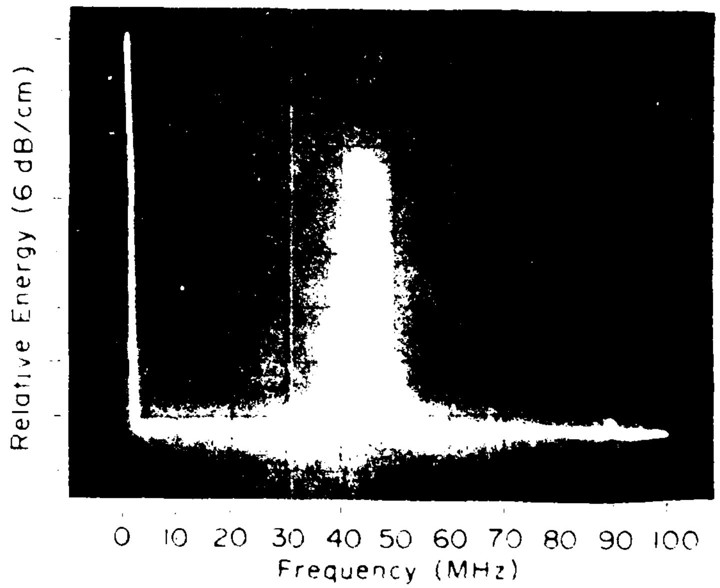


Fig 15 2C DAMPED SINUSOID SPECTRUM

A pulser with a rise time of less than two (2) nanoseconds shall be used, e.g., the HP215A. The pulsewidth is set equal to the rise time of the desired double exponential envelope. For general testing, this shall be 10 ns as shown in the figure.

This pulse is then passed through a simple pulse-shaping network to obtain the double exponential envelope. The capacitor shall be chosen to provide an RC time constant that reduces the amplitude of the damped sinusoid to 50% of its peak amplitude within 5 to 10 cycles of RF. The diode shall be a high speed device such as an HP hot carrier diode.

The envelope pulse is amplified and inverted with a broadband RF preamplifier, such as the HP462A.

Finally, a double-balanced mixer, such as the Minicircuits ZAY-1, is used as a modulator, thus providing damped RF sinusoids at its output.

Figure 15.3A illustrates the test setup for generating RF bursts. Figures 15.3B and 15.3C illustrate a typical waveform and spectral distribution, respectively. This waveform is simpler to generate and is suitable for upset testing. It is not preferred for damage testing, however, as this waveform contains more energy for a given amplitude than does the more realistic damped sinusoid waveform.

In this setup the RF generator, optional trigger and double-balanced mixer are used in the same manner as previously discussed. The main difference is that the output of the pulser is used directly to modulate the RF. The pulse amplitude is to be approximately 1 volt and the pulse duration shall be between 5 and 10 RF cycles. As in the previous setup, a low duty cycle is recommended. Hence, a repetition rate of 1 kHz should be used.

15.2.2.3 Precautions

Double-balanced mixers are linear only over a small range of input amplitudes. Thus, the envelope of the damped sinusoid

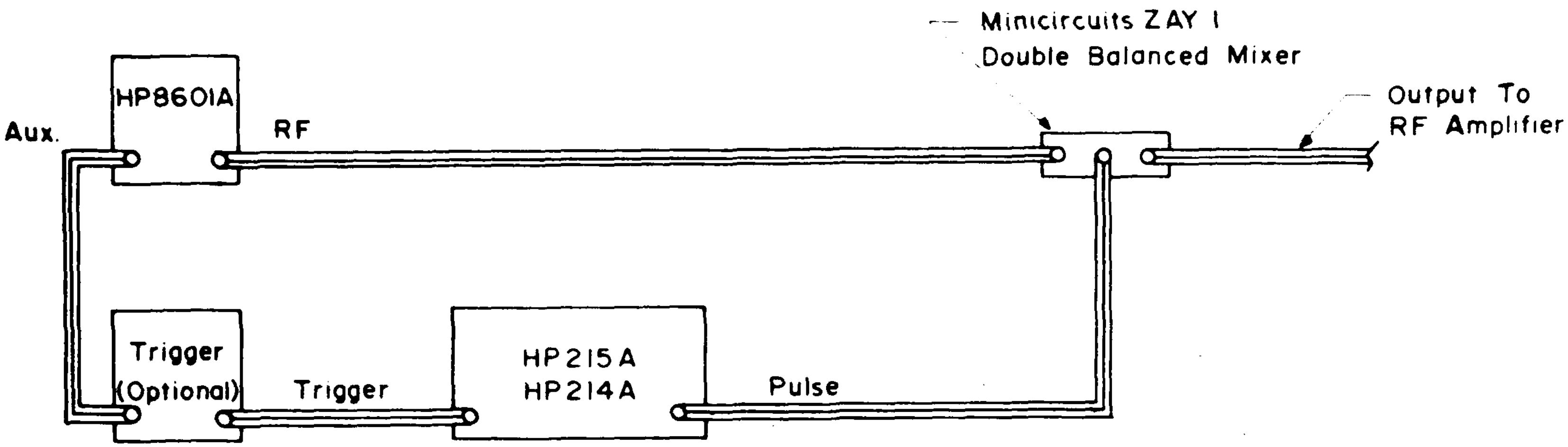


Fig. 15.3A TYPICAL TEST SET-UP FOR GENERATING RF BURSTS

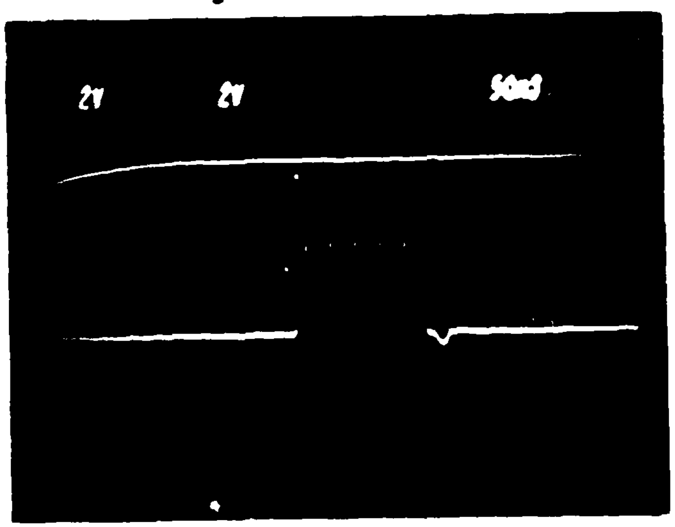


Fig. 15.3B RF BURST WAVEFORM

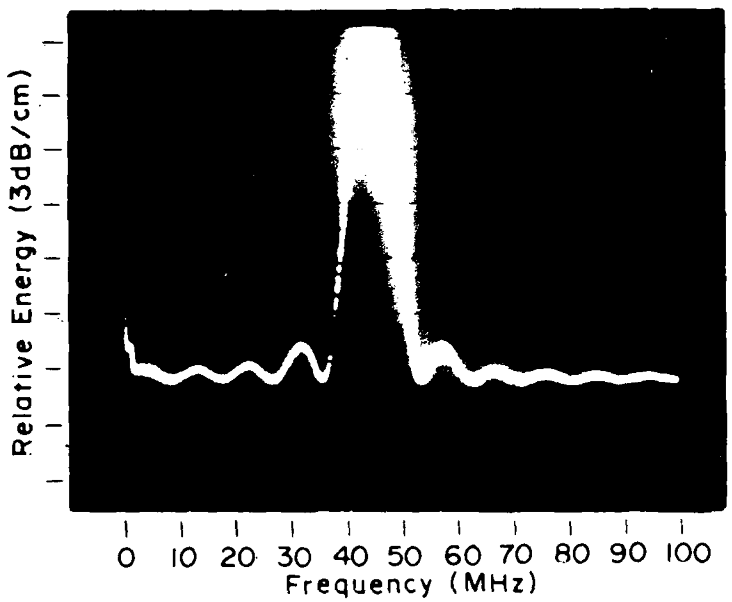


Fig. 15.3C RF BURST SPECTRUM

output will not be identical to the modulating envelope. Prior to the start of testing it will be necessary to adjust the amplitude and duration of the modulating envelope in order to achieve the desired output.

Some portion of the simulated EMP current will flow toward the load rather than toward the unit under test. In general, the load impedance and the cable impedance will not be matched, so reflections will occur. Thus, in order to avoid misinterpretation of the signal observed at the module terminal, it is important that the test system be configured in a manner that takes these reflections into account. This may be accomplished by making the cable very long so that the reflections do not return during the time the terminal is being observed, or by making the cable very short so that the reflected and direct signals are very nearly coincident. Since it is convenient to be able to view the unit under test-cable-load as a lumped parameter system, the short cable approach is preferred. Thus, to insure that the round trip transit time on the cable is short compared to the 10 ns EMP rise time, the cable length should be limited to two feet.

Ground loops must be avoided. One source of trouble is grounding via instrument power line cords, particularly if the unit under test is powered by ac. To avoid such loops, the chassis grounds for both the instruments and the unit under test should be floating from ac ground.

15.2.2.4 Data Format

There are basically two types of raw data to be recorded. One is data describing the EMP transient introduced into the terminal. The voltage at and current into the terminal are to be recorded. Polaroid pictures of the oscilloscope display will be suitable. The second type of data is that which describes the effects of the EMP transient. The test engineer must be responsible for determining the most suitable means of recording this information since the test engineer is the one who defines what effects are to be measured.

This data shall be reduced to a meaningful format, preferably graphical. Generally, it is best to graph the minimum transient voltage/current/power/energy versus the log of frequency required to produce a given effect. For example, Figure 15.4 illustrates the minimum voltage required to upset a digital integrated circuit versus the log of frequency. This example is for a qualitative effect (i.e., either upset or not upset). Quantitative effects (i.e., percent distortion, energy of spurious output, etc.) should be presented as a family of curves; each curve for a different amplitude or degree of effect.

When testing to a given specification, it is possible that specification-level pulses will produce no significant effects for some or all of the terminals (i.e., some or all of the terminals are not susceptible to the given EMP). This information should be presented in a tabular format with appropriate raw data appended.

15.3 Module Testing Without Specification

15.3.1 Applicability

The purpose of this type of testing is to assess the overall hardness of a module to cable-coupled EMP transients, as opposed to the tests in the previous section which are designed to validate a particular module to a given specification. This type of testing is applicable to testing programs with any of the following objectives:

- Providing EMP hardness data for comparing competitive modules;
- Providing data for the design of terminal protection;
- Determining EMP "safety margins" provided by terminal protection.

It is recommended that both the CW Test and the Direct Pulse Injection Test be performed.

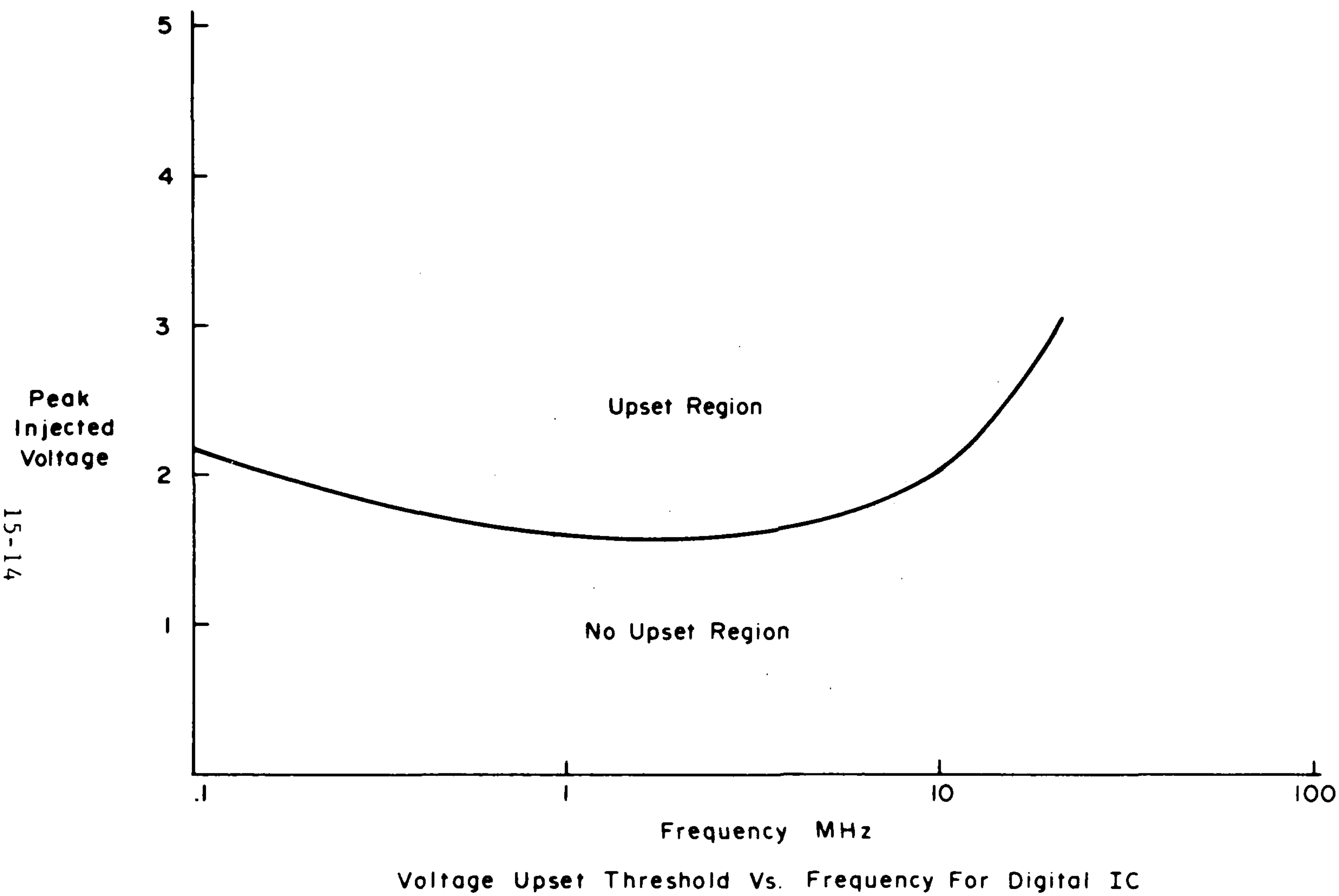


Fig. 15.4 EXAMPLE DATA FORMAT FOR DIRECT INJECTION TESTING

4 The CW Test is not an EMP test. Rather, it is used to measure the input impedance of each pin versus frequency, and to measure terminal-to-terminal transfer functions as necessary. The data from these measurements will be used by the test engineer to aid in selecting test frequencies for the direct pulse injection test, i.e., the CW test determines critical test frequencies such as minimum impedance points, maximum impedance points and resonance points.

For both of these tests, pin-to-case injection is recommended. In the case of differential signals, pin-to-pin injection shall also be used. Every pin should be tested except in cases of extreme redundancy, such as a computer data bus. In such cases it is necessary to test only two or three lines to insure that the effects are the same for all.

15.3.2 CW Test Procedure

15.3.2.1 Scope

CW tests are used to measure the impedance versus frequency of the module terminals and to measure the transfer function between two terminals versus frequency. The results of these tests are useful for selecting test frequencies for direct injection testing of EMP transients.

15.3.2.2 Test Equipment

Figure 15.5 illustrates the test setup for measuring the terminal impedance versus frequency. This requires a swept frequency generator and a network analyzer such as the Hewlett-Packard 8601A and 8407A, respectively. The current probe is connected to the reference channel and the voltage probe to the test channel. Connected in this fashion, the network analyzer subtracts the logarithm of the terminal current from the log of the terminal voltage and displays the log of the terminal impedance. Some units, such as the 8407A, also display phase.

Figure 15.6 is an example of a test setup to measure the transfer function between two terminals. In this case, a power splitter is required to obtain the reference signal.

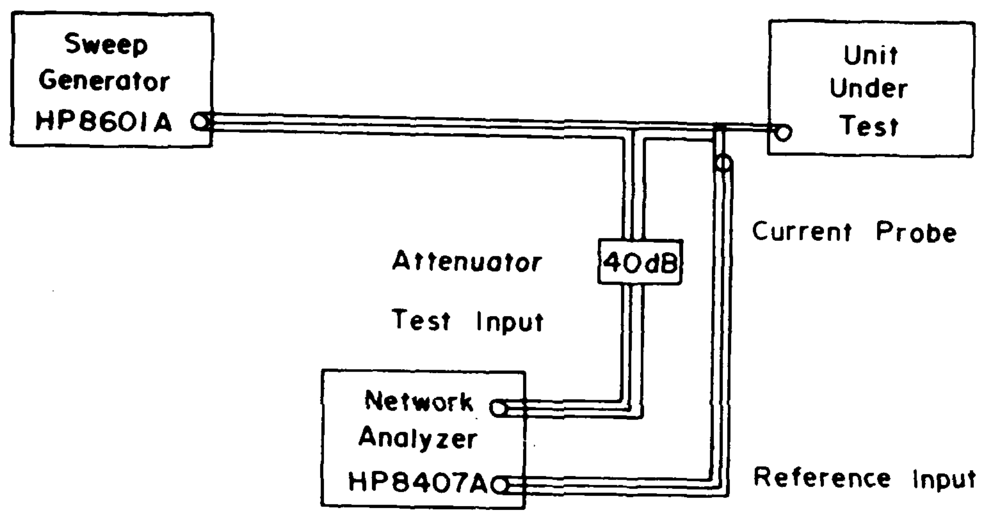


Fig. 15.5 SWEPT FREQUENCY TERMINAL IMPEDANCE MEASUREMENT TEST SET-UP

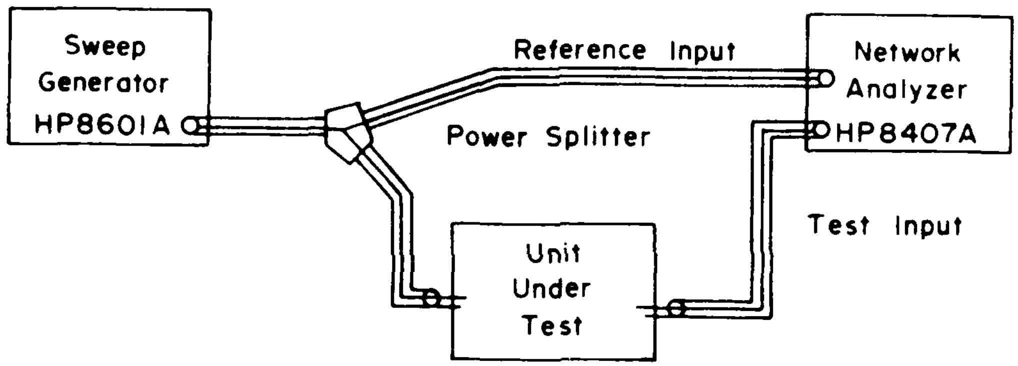


Fig. 15.6 SWEPT FREQUENCY TRANSFER FUNCTION MEASUREMENT TEST SET-UP

15.3.2.3 Precautions

The test equipment must be calibrated. The basic calibration is to replace the unit under test with a 50 Ω termination as shown in Figure 15.7. The network analyzer is then adjusted to read 50 Ω and 0^{o} of phase angle at low frequencies. The response should be flat over the full working range of frequency. Where this is not the case, simple corrections can be applied to the recorded data.

The input impedance of the terminals is to be measured both with the module energized and turned off. When energized, it will be necessary to provide dc blocking capacitors if dc is present on the terminal. The impedance of digital output circuits should be plotted in both the high and low states.

15.3.2.4 Data Format

The basic data to be recorded are the magnitude and phase of the terminal impedance, Z_T, as a function of frequency. Measurements should be made over a three decade frequency range from 100 kHz to 100 MHz. Polaroid pictures of the network analyzer display will be suitable. Figure 15.8 shows the magnitude and phase of the terminal impedance for the output terminal of the HP462A amplifier. Note the spaces provided to identify the unit under test, test setup, terminal and test conditions. In this case, the test was performed with power on, as indicated in the figure.

Not all terminals have impedances as well behaved as are those of the HP462A. Figure 15.9 shows the terminal impedance of a digital output driver in its low state. Note the resonance points, especially the sharp dip at 2 MHz. When present, such resonance points should be noted for future use as they will be specifically selected as test points in the direct injection test.

15.3.3 Direct Pulse Injection Test Procedure

This test is the same as that of Section 15.2.2. The only

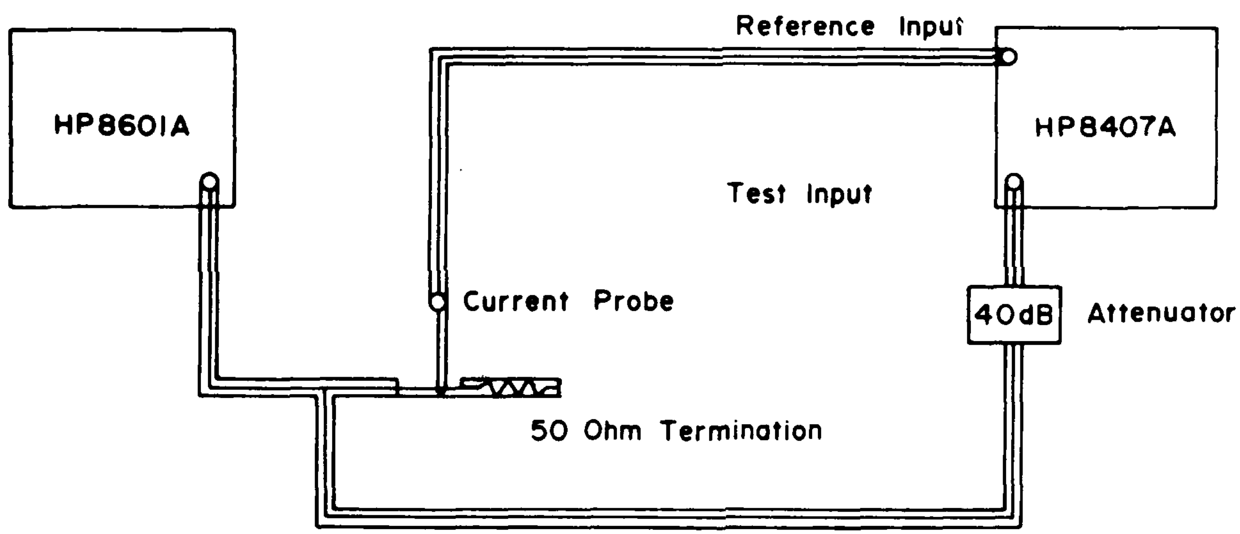


Fig. 15.7 CALIBRATION OF SWEPT FREQUENCY SYSTEM

UNIT UNDER TEST [illegible] Amplifier
TERMINAL(S) Output [illegible]
DATE [illegible]

Bright Trace

Display [illegible]

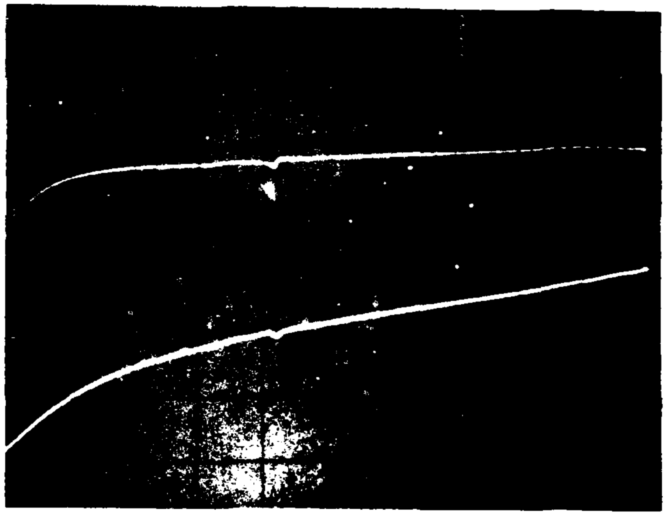
Amplitude [illegible]

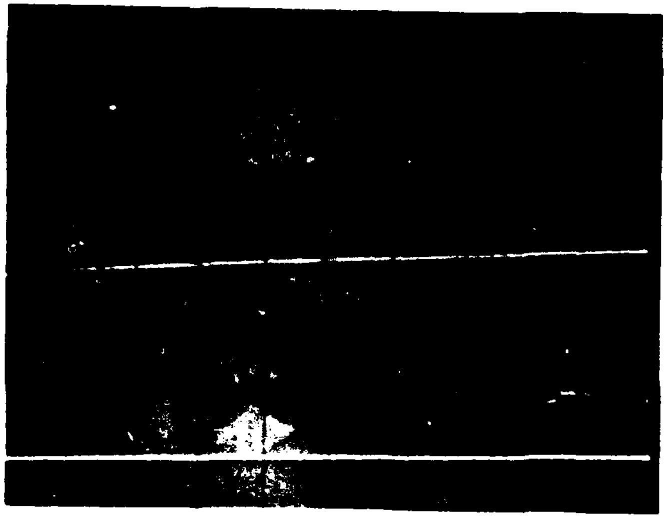
Dim Trace

Phase [illegible]

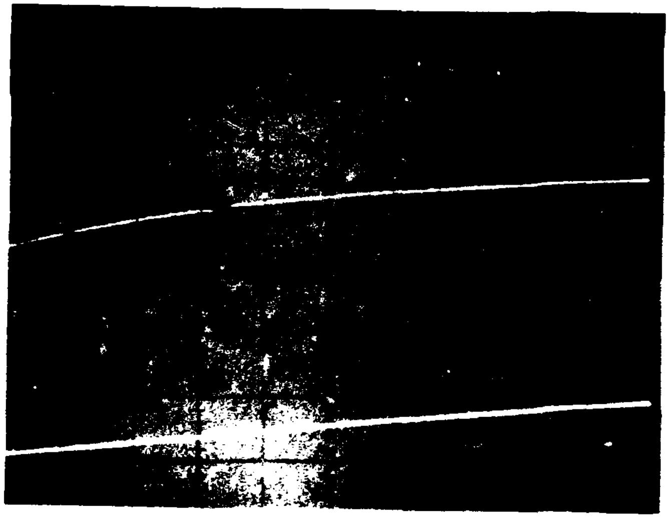
Phase [illegible]

NOTE Gain control - [illegible]





[illegible] to [illegible]



[illegible]

Figure [illegible]

UNIT UNDER [illegible]
TERMINAL(S) [illegible]
DATE Oct. [illegible] [illegible]

Bright Trace

Display Ref [illegible] dB [illegible] center

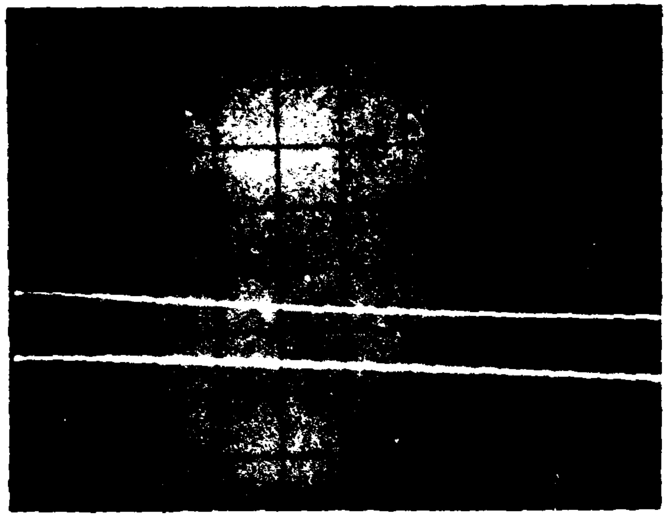
Amplitude [illegible] dB [illegible]

Dim Trace

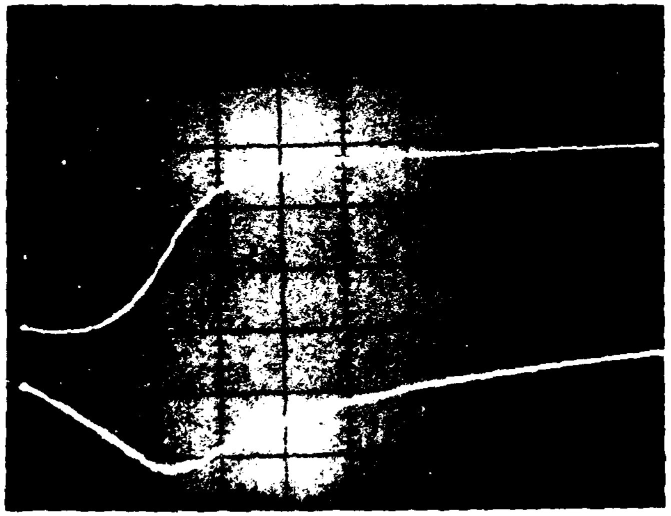
Phase Offset [illegible] center

Phase [illegible] div [illegible]

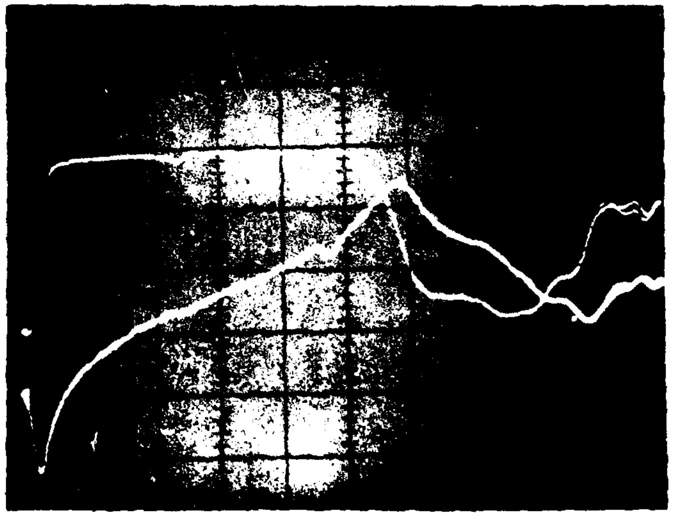
NOTE: Power On



0.1 to 1.1 MHz



1.0 to 11.0 MHz



[illegible] MHz

Figure [illegible]

difference is in the selection of test pulse frequencies and amplitudes.

For module testing without a specification, the Direct Pulse Injection Test shall be executed at a minimum of 12 frequencies, i.e., four test frequencies per decade between 100 kHz and 100 MHz. The resonance points determined by the CW test shall be among these frequencies.

Test pulse amplitudes should range from a level which causes no significant effects to the level that causes module destruction.

15.4 Acceptance/System Level Testing

15.4.1 Applicability

The purpose of this type of test is to verify the overall hardness of a module or a modular system to a specified EMP. While it would be ideal to expose the entire system to a free field, threat level EMP simulator to perform this type of test, such an approach is not always practical or feasible, nor is such a simulator always readily available to the test engineer.

In such cases it is recommended that the Bulk Injection Test be utilized. Typical applications of this test include:

- Quality assurance testing of modules;
- Field testing;
- Testing interfaces between systems, i.e., umbilical between aircraft and aircraft carrier;
- System acceptance testing when use of free field simulators is not practical.

This type of testing (simulator or bulk injection) is very popular, as it provides for current distribution within the system, reflections at interfaces and possible synergistic effects due to simultaneous pulses arriving on several pins. Such testing is intended as a benchmark, a final verification

to account for effects not easily simulated by other methods. Since system configurations are changed with time an overall testing program should utilize this type of test in addition to and not in place of the more detailed tests discussed earlier.

15.4.2 Bulk Injection Test Procedure

15.4.2.1 Scope

Bulk injection tests are used to determine the gross effects of EMP transients on electronic modules or entire systems, by injecting a specified bulk current on the interconnecting cable(s). This current distributes among the individual conductors according to the impedances which terminate the conductors. Thus, every pin in the associated interface is tested simultaneously. If data is required for individual pins, it is recommended that the direct injection test, Section 15.2, be used.

15.4.2.2 Test Equipment and Setup

In bulk injection testing, there are two techniques for coupling the simulated EMP to the interconnecting cable(s), i.e., inductive and capacitive. Both of these techniques provide loose coupling between the pulser and the unit under test, and therefore do not alter the normal operation of the unit under test. In either case, it is recommended that the damped RF sinusoid waveshape be used for simulating the EMP. The magnitudes and frequencies for the bulk current transients are to be specified by the Program Office for the system in which the module is being used.

For laboratory testing, either coupling technique is suitable. For in-situ testing on actual systems, however, inductive coupling is preferred due to the relatively small size of the coupling transformer and because these transformers may be clamped around the cable being tested without disconnecting the cable. Figure 15.10 illustrates the typical test setup for performing bulk injection with inductive coupling.

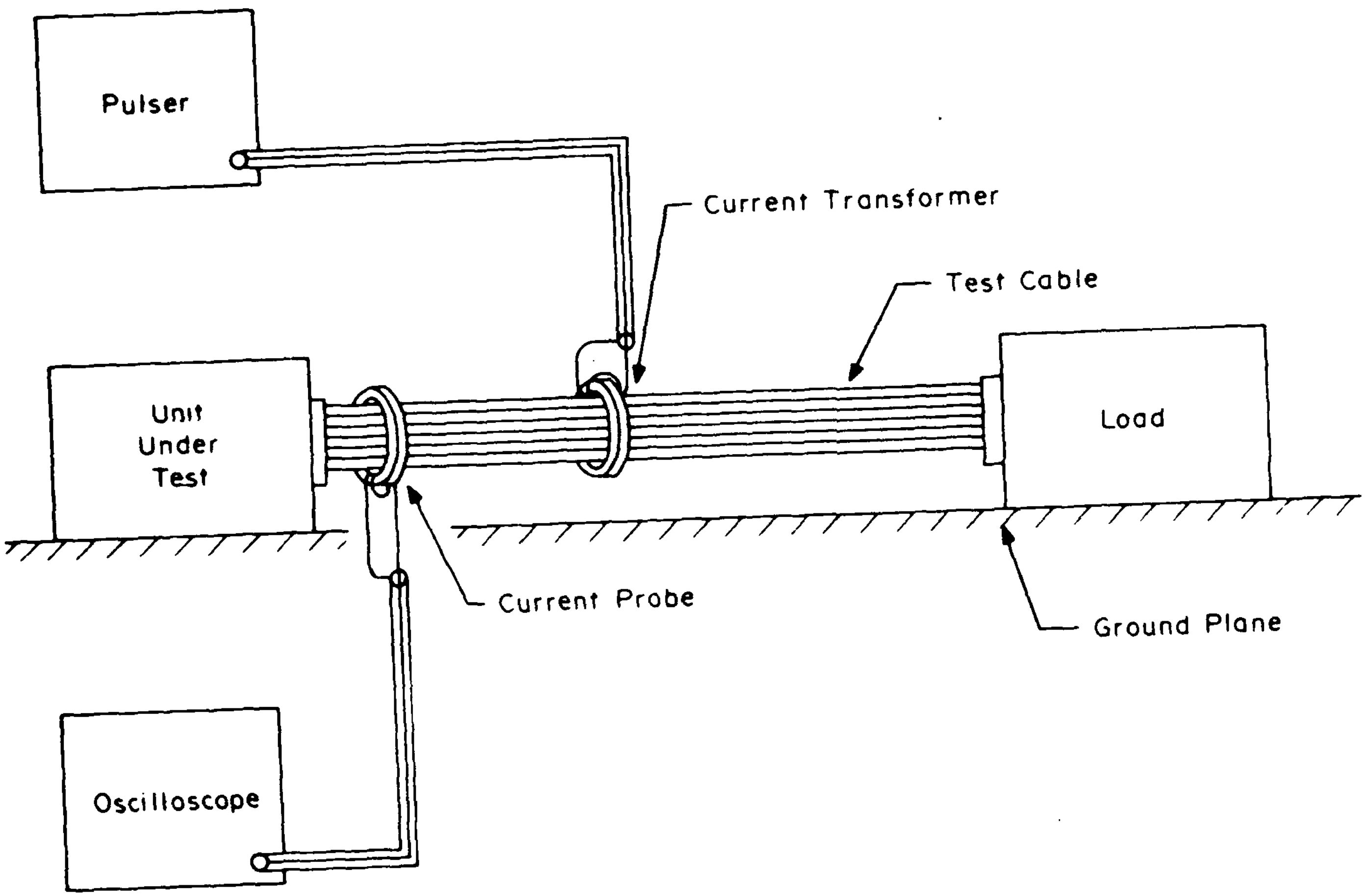


Fig. 15.10 BULK INJECTION TEST SETUP WITH INDUCTIVE COUPLING

This technique utilizes a current transformer to couple energy from the pulser to the cable. These transformers must be carefully designed to deliver the required current without going into saturation.

Because of the loose coupling technique being utilized, the pulser must be capable of generating damped RF sinusoid pulses at very high power levels. These pulses may be generated by the same method described in Section 15.2.2.2. To achieve the desired bulk current, however, the power requirement on the broadband RF amplifier will generally be in excess of 1 kw. Alternately, a high voltage capacitive discharge type pulser may be used.

The current at the terminal of interest should be monitored with an oscilloscope. A broadband current probe, such as the Stoddart 91550-1, will be required.

The module is to be tested in an operational state, i.e., energized and functioning. Thus, it is necessary to terminate the cable from the unit under test. This termination is also required to insure that the bulk current distributes correctly among the cable conductors. Ideally, the actual unit(s) that would terminate the cable in a real system should be used as the load. This generally is possible when performing in-situ tests on a real system, but is often impossible when performing laboratory tests, since the actual load units may be unknown, unavailable or sensitive to EMP. In such cases, it is necessary to simulate the actual or anticipated load impedances, voltage levels, control signals, etc., to the unit under test. Load impedances generally may be simulated with simple passive networks. The simulation of voltage levels or control signals, however, requires the attention of someone familiar with the unit under test.

For laboratory testing, the unit under test and the load shall be affixed to a common ground plane to provide a low impedance return for the injected current. For in-situ testing

of modules affixed to metallic structures (i.e., ships, aircraft, etc.), this is unnecessary since the structure will provide a return path.

Figure 15.11 illustrates some typical RF burst voltage and current waveforms injected on a computer data bus with the inductive coupling technique. These traces were redrawn from oscilloscope photographs to improve clarity. The waveforms appear only as envelopes in the photographs so the phase relationships in the figure may be incorrect. Note that this is not the recommended waveform for EMP testing and is used here only as an example.

Figure 15.12 illustrates a typical test setup for bulk injection with capacitive coupling. In this technique, the pipe acts as one plate of a capacitor and the cable conductors form the other plate. The pipe should be 4 to 8 feet long and several inches in diameter.

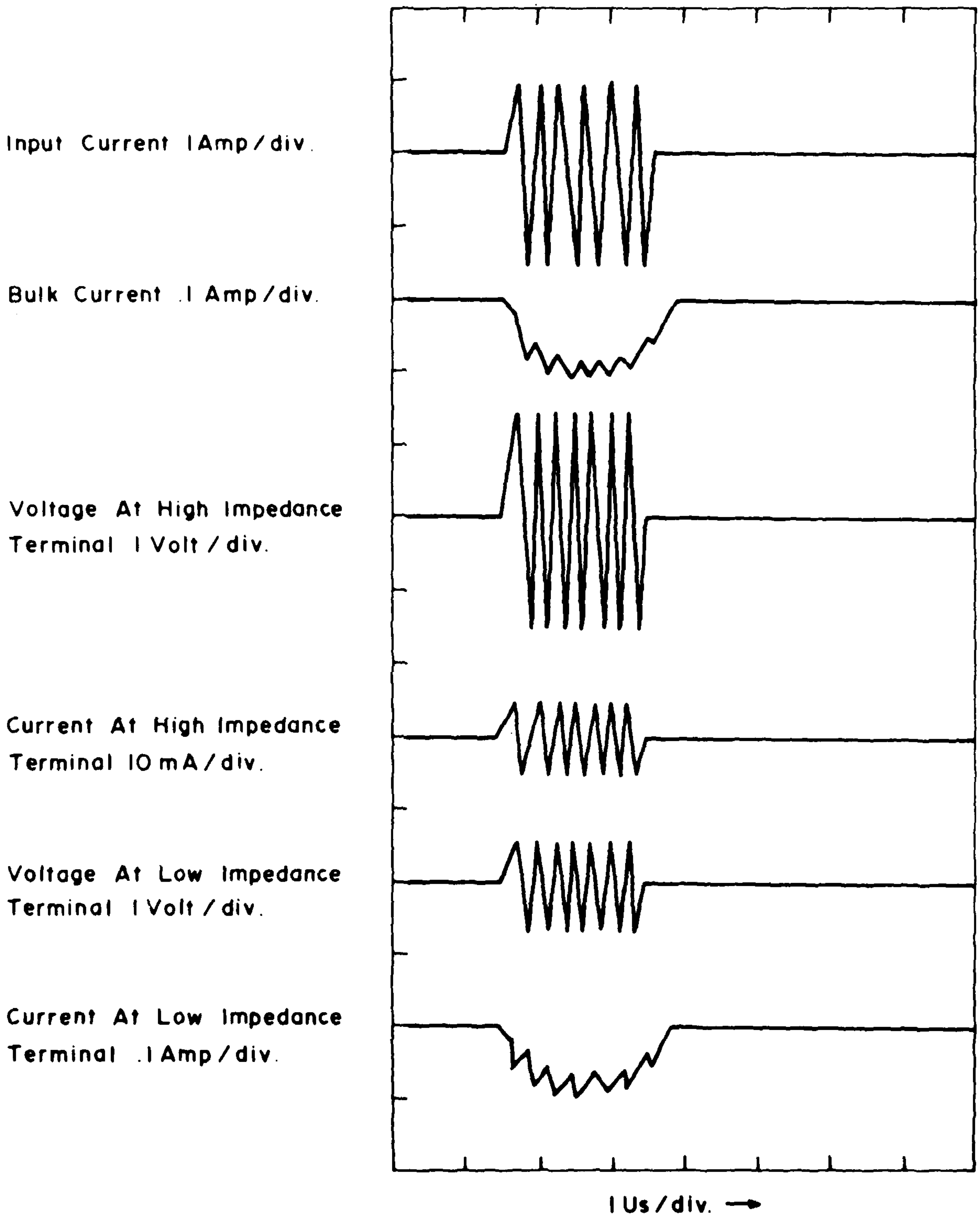
Since the pipe over the ground plane forms a section of transmission line, the pipe must be terminated with resistor R_T to prevent ringing.

Except for the coupling technique, this test setup and the previous test setup are the same.

15.4.2.3 Precautions

Since the simulated EMP is coupled to the system via the test cables, the construction and shielding of the test cables are to be the same as the construction and shielding of the actual or anticipated system cables. Some important factors are the following:

- Are signals carried on twisted pairs or individual leads?
- What is the number of ground leads?
- Is the cable shielded?
- Is shielding braided or solid?



Note: Phase Relationships May Be Incorrect

Fig. 15.11 REPRESENTATIVE BULK INJECTION WAVEFORMS

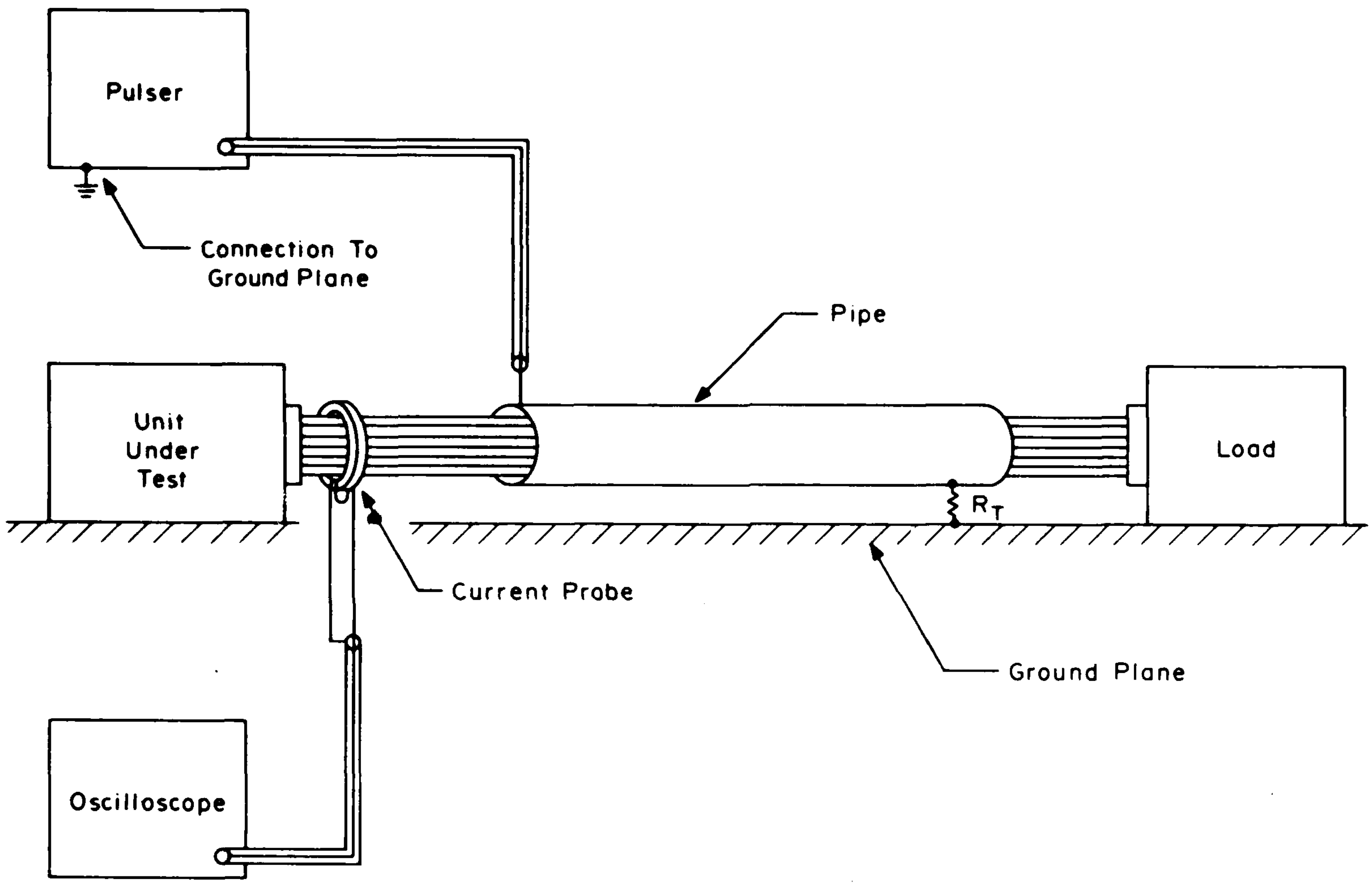


Fig. 15.12 BULK INJECTION TEST SETUP WITH CAPACITATIVE COUPLING

Improper grounding can be a source of significant errors. When performing laboratory tests it is important that the unit under test and the load be affixed to a common, low impedance ground plane. This is generally not necessary when performing in-situ tests in which case the current is allowed to return via the natural path(s).

The test engineer must be careful to insure that the instrumentation is not detecting false signals, i.e., picking up cross-talk between cables or detecting radiated energy. This is a particular problem when performing bulk testing because of the high power level being used. Often it is necessary to locate the instrumentation in a shielded enclosure to prevent radiated energy from interfering with the measurements. All cables between the instrumentation and the test setup must be well shielded or optical data links may be used.

15.4.2.4 Data Format

There are basically two types of raw data to be recorded. One is data describing the bulk current introduced into the terminal. Polaroid pictures of the oscilloscope display will be suitable. The second type of data is that which describes the effects of the EMP transient. The test engineer must be responsible for determining the most suitable means of recording this information since the test engineer is the one who defines what effects are to be measured.

This data shall be reduced to a meaningful format. Bulk injection testing is often used to perform pass/fail tests. Such information may be presented in a tabular format showing frequency, current and pass/fail for each test point. Raw data should be appended or at least retained in good order by the test engineer. Alternately, it may be necessary to provide data that indicates at what level of bulk current a particular effect occurs. This information should be reduced to a graphical format which plots the minimum bulk injection current required to produce a given effect versus the log of frequency.

For example, Figure 15.13 illustrates the minimum bulk current required to cause upset on a computer interface versus the log of frequency. This example is for a qualitative effect (i.e., either upset or not upset). Quantitative effects (i.e., percent of distortion, energy of spurious output, etc.) should be presented as a family of curves; each curve for a different amplitude or degree of effect.

15.5 Additional Considerations for Testing Digital and Special Analog Modules

Digital modules will possess some or all of the following characteristics:

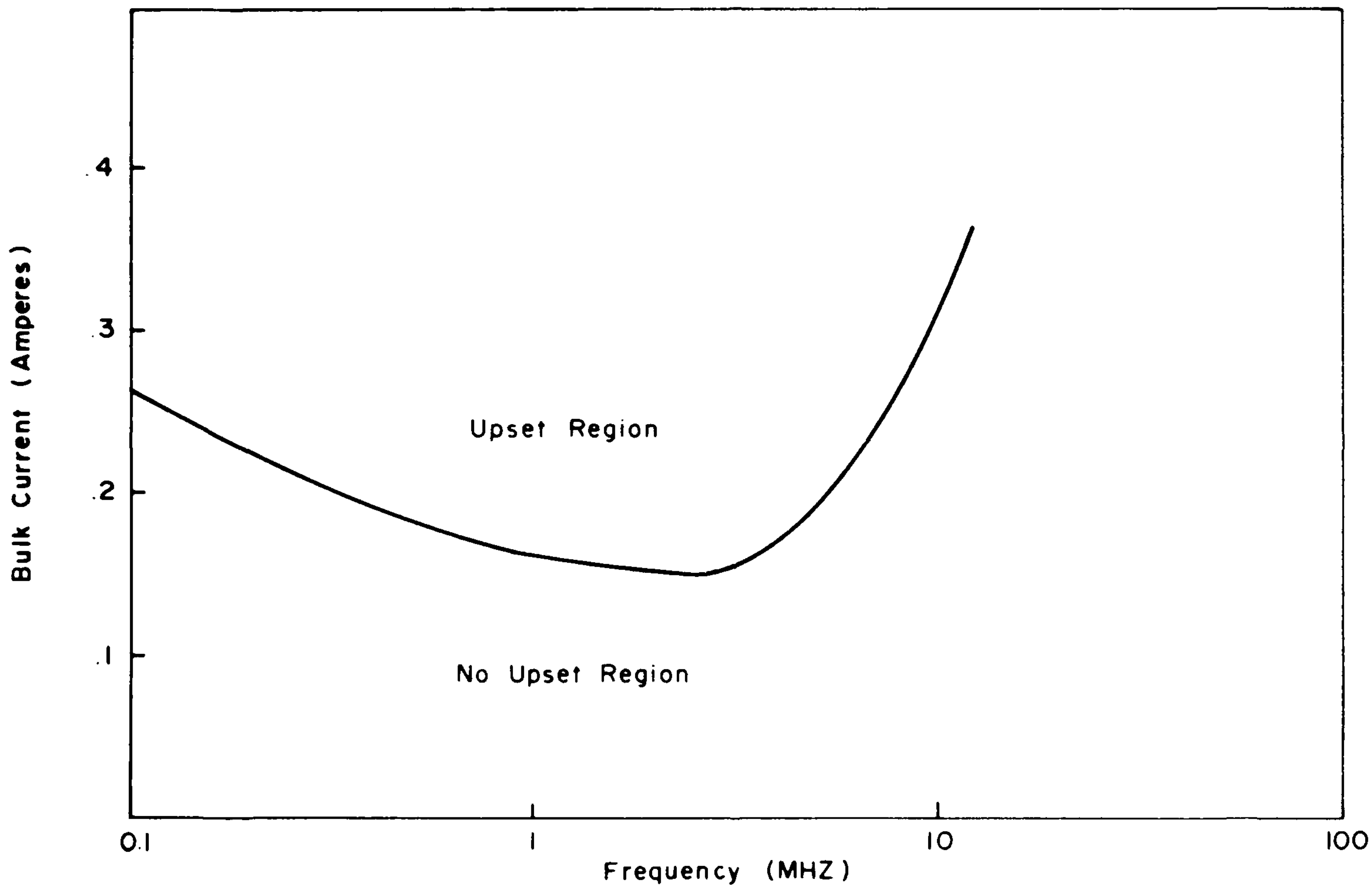
- Input/output impedance which is nonlinear with input/output voltage;
- Numerous states with potentially different levels of sensitivity;
- Memory.

Some analog devices, such as FET analog switches, also possess some of these characteristics and shall be treated accordingly.

Three topics are considered in this section:

- Techniques for simulating digital loads;
- Techniques for synchronizing pulse delivery with operation of a multistate machine;
- Use of software in testing.

In both the Direct Pulse Injection Test and the Bulk Injection Test it is important that the test cables be terminated in actual or simulated loads. While actual loads are preferred, simulation is often necessary. Since digital devices exhibit different impedances in the high and low states, it is required that each terminal be tested high and low. For upset testing, the simplest approach is to construct a dummy load module utilizing switches and standard interface gates for the



Bulk Current Upset Threshold Vs. Frequency For Computer I/O Bus

Fig. 15.13 EXAMPLE DATA FORMAT FOR BULK INJECTION TESTING

appropriate logic family. Figure 15.14 illustrates this method as applied to the TTL family. If damage level testing is being done, a more durable load should be constructed from discrete components. Generally, the manufacturer's literature will provide schematics for such circuits. Figure 15.15 illustrates this approach. The devices shall be selected with breakdown voltages higher than those of the interface devices in the unit under test.

Figure 15.16 illustrates, in block form, the concept of synchronizing the pulser with operation of a multistate unit under test. For units with hard wired logic, i.e., modules which do not operate under software control, a suitable signal from the unit under test may be buffered and used to trigger the pulser. If no such signal exists, it is necessary to decode some combination of signals within the unit which define the state to be tested. Care must be taken to avoid creating a ground loop. If the control signal(s) must be carried over a distance of more than a few feet, an optical fiber link is recommended.

When testing computers, i.e., modules which operate under software control, many additional tests are available.

Two unique methods of triggering the pulser are available. One is to utilize an idle interface to control triggering the pulser. An output instruction, directed to the unused terminal, will trigger the pulser. This allows complete program control over delivery of the simulated EMP. This approach is similar to that described in Figure 15.16, and is used in the program segment in Figure 15.17. Alternately, an advanced trigger from the pulser can be used to interrupt the computer and cause it to branch to the appropriate test routine. Naturally this latter technique applies only to computer with interrupt handling features. For single shot testing, either method is equally applicable.

For upset testing, however, the former method is more

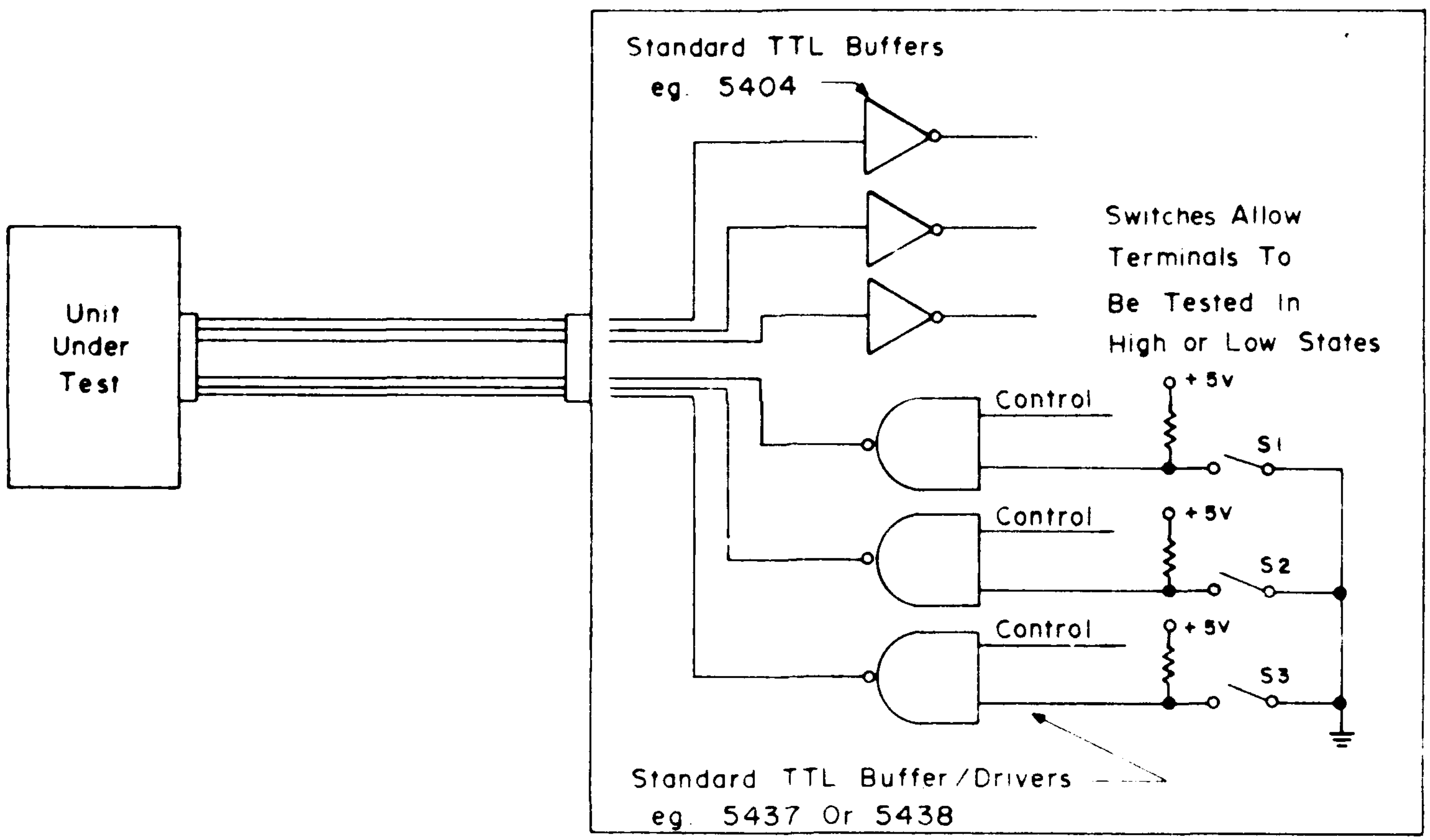


Fig. 15.14 TYPICAL SIMULATED DIGITAL LOAD FOR UPSET TESTING

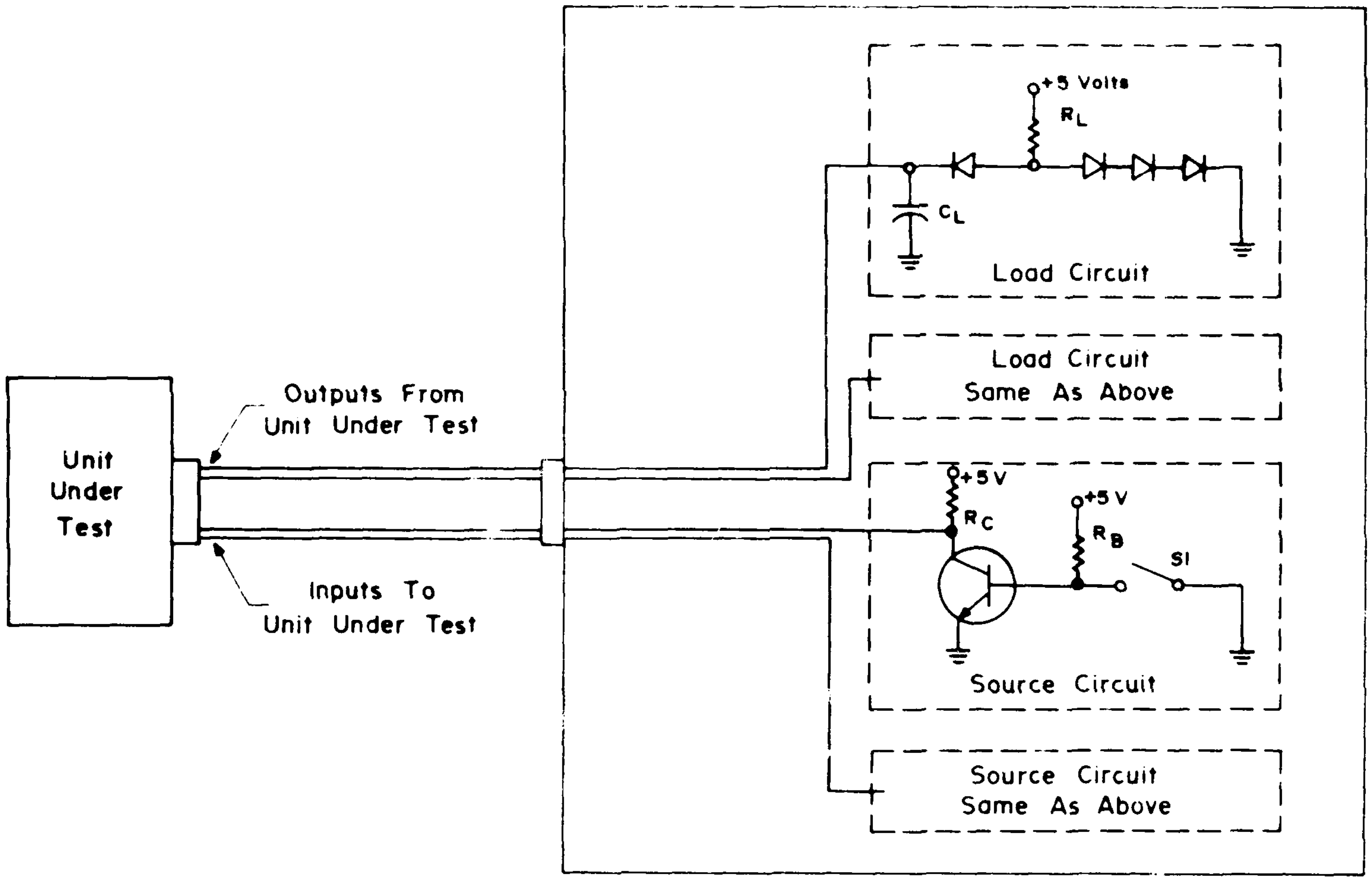


Fig. 15.15 TYPICAL SIMULATED DIGITAL LOAD FOR DAMAGE TESTING

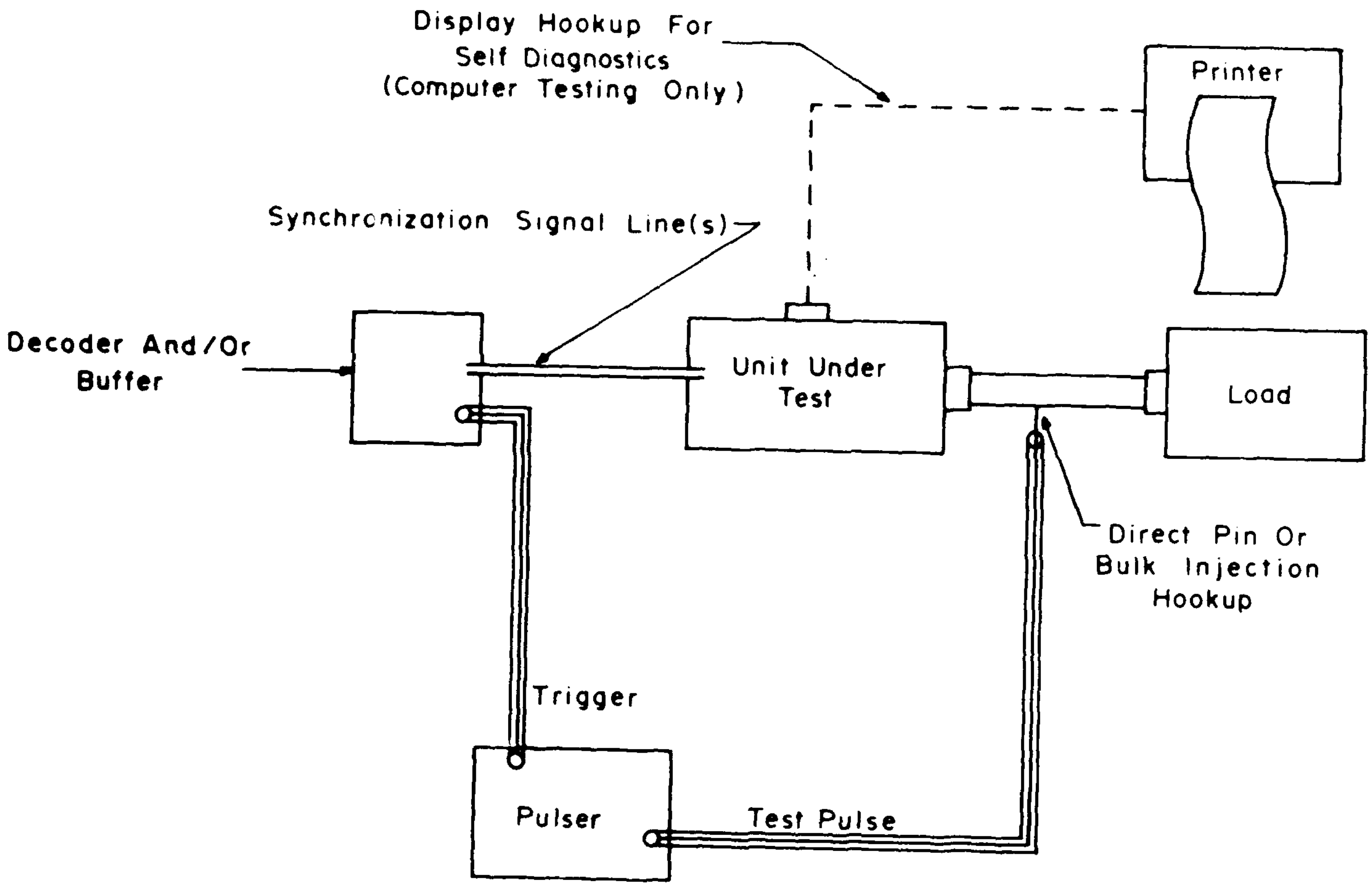


Fig. 15.16 SYNCHRONIZING PULSER WITH OPERATION OF MULTISTATE MODULE

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```
0001  .MAIN
      005000          .LOC 5000
                                            ;TELETYPE TEST ROUTINE
05000 062677          START:  IORST
05001 152440                  SUBC    2.2       ;CLEAR AC2
05002 020476                  LDA     0.EXC     ;LOAD " CODE INTO AC0
05003 176440          TST1:   SUBO    3.3       ;CLEAR AC3
05004 054520                  STA     3.TSTF    ;CLEAR TEST POINTER
05005 060352                  NIOP    52        ;SEND TRIGGER PULSE
05006 070510                  DIAS    2.TTI     ;READ A CHARACTER FROM TAPE     First Emp Is Triggered Here ...
05007 063510                  SKPBZ   TTI       ;DONE READING?                  ... And Arrives Here
05010 000777                  JMP     .-1       ;NO.WAIT UNTIL DONE...
05011 151005                  MOV     2.2.SNR   ;BLANK CHARACTER?
05012 000772                  JMP     .-6       ;YES.READ ANOTHER
05013 0[illegible]            LDA     1.ONE     ;SET TEST POINTER...
05014 044510                  STA     1.TSTF    ;TO TEST 1....
05015 126440                  SUBO    1.1       ;AND CLEAR ACC
05016 004442                  JSR     CK1       ;GO CHECK CHARACTER             Check For Upset
                              ;TEST MEMORY LOAD FROM AC2.
05017 060352          TST2:   NIOP    52        ;SEND TRIGGER PULSE
05020 050457                  STA     2.SAV     ;LOAD CHARACTER INTO MEMORY     Second Emp Is Triggered Here ...
05021 0[illegible]            ISZ     TSTF      ;SET TEST POINTER 2             ... And Arrives Here
05022 004442                  JSR     CK2       ;GO CHECK CHARACTER             Check For Upset
                              ;TEST AC2 LOAD FROM MEMORY.
05023 060352          TST3:   NIOP    52        ;SEND TRIGGER PULSE
05024 030453                  LDA     2.SAV     ;RESTORE CHAR. TO AC2           Third Emp Is Triggered Here ...
05025 0[illegible]            ISZ     TSTF      ;SET TEST POINTER=3             ... And Arrives Here
05026 004430                  JSR     CK1       ;GO CHECK CHARACTER             Check For Upset.
                              ;ALL CHECKS GOOD...GET NEXT CHARACTER
05027 030453                  LDA     2.Z       ;LOAD Z INTO AC2
05030 112415                  SUB#    0.2.SNR   ;SKIP NEXT IF CHAR NOT Z
05031 000403                  JMP     DONE      ;CHAR=Z...TEST COMPLETE
05032 101400                  INC     0.0       ;FORM NEXT CHAR IN SEQUENCE
05033 000750                  JMP     TST1      ;...AND START OVER
05034 024441          DONE:   LDA     1.PASSX   ;LOAD AC1 WITH MSG ADDRESS..
05035 004410                  JSR     MESG      ;...GO TO OUTPUT SUBROUTINE
[illegible]                   [illegible]       ;[illegible] RESPONSE
[illegible]                   JMP     START     ;[illegible]
```

Fig 15.17 SAMPLE PROGRAM SEGMENT FOR EMP TESTING OF COMPUTER

suitable. Since the pulser is under program control, a series of pulses can be utilized with the computer halting only when an upset condition is detected. The test may then be repeated at the upset level on a single shot basis and the waveforms recorded. This approach will save a significant amount of time over a strictly single shot method.

In either case, diagnostic software should be utilized to detect and perhaps isolate the upset or damage. Such programs are constructed using instructions which exercise the circuitry or operation under investigation. The program segment in Figure 15.17 is an example which illustrates the basic approach to diagnostic testing. The instruction "NIOP 52" generates an output signal to trigger the pulser as discussed above. Thus, the simulated EMP will always occur during the instruction immediately following the NIOP 52. In this example, we are testing the instructions at locations 5006, 5020, and 5024 which are input from teletype, load memory from register and load register from memory respectively. The data input/loaded is always predefined and after each EMP the register or memory location under consideration is checked. If the contents are not correct, an error message is output to the display, otherwise the test is repeated. After approximately 50 repetitions, the computer will output a pass message and halt, allowing the technician to increase power, change frequency, etc., before resuming the test.

The example tests only three of the computer's instructions. Figure 15.18 illustrates the timing of the three trigger pulses generated by the program. In an actual program, however, it will be necessary to test many different instructions such that a reasonable cross-section of the computer's possible states are examined.

Simulated EMP

Timing Pulse
From Computer

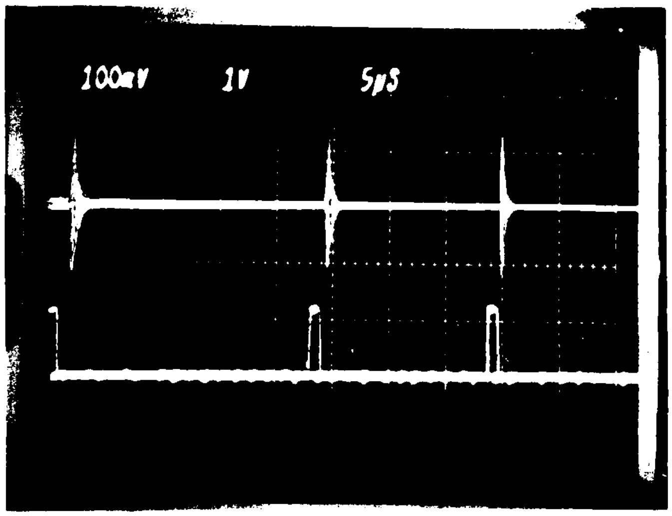

Fig. 15.18 EXAMPLE OF TIMING FOR SYNCHRONIZED PULSING

15.6 References

W. E. Boettcher, <u>et al</u>., <u>Electromagnetic Pulse Handbook for Missiles and Aircraft in Flight</u>, (Albuquerque, New Mexico: Sandia Laboratories, 1972). pp. 271-276. (SC-M-710346)

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